Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application;

Listing of Claims

Claim 1 (Currently amended): A binary digits coding method, comprising a step of transforming a series of binary digits generated from binary digits "0" and "1" into a sequence of pulse groups, wherein the binary digits "0" and "1" in the series of binary digits are transformed respectively into two pulse groups which have two different special defined pulse frequencies and have ~~the~~ same defined number of pulses thereby having different duration times, and said defined number is at least two.

Claim 2 (Currently amended): A decoding method for transforming a sequence of pulse groups into a series of binary digits generated from binary digits "0" and "1", the sequence of pulse groups comprising of pulse groups which have two different special defined pulse frequencies and have same defined number of pulses thereby having different duration times, said defined number being at least two, the decoding method comprising ~~comprising steps of~~:

dividing the sequence of pulse groups into pulse groups according to the same defined number of pulses;

measuring duration times of the pulse groups ; and

transforming the pulse groups into binary digits "0" or "1" according to the different duration times of the pulse groups.

Claim 3 (Original): The decoding method as set forth in claim 2, wherein the said duration time of the pulse group is the total time of the period time of the all the pulses in the group,

or is the sum of the period time of part of specially defined pulses in the pulse group.

Claim 4 (Currently amended): A digital signal transmission method, including a process of sending and transferring binary signals generated from binary digit signals "0" and "1" from a transmission side to a reception side, wherein, ~~a~~

at ~~t~~ the transmission side, the binary signals ~~digits~~ are expressed as a sequence of pulse groups; the ~~digits~~ binary signals "0" and "1" are expressed by two pulse groups with two special pulse frequencies and with same defined number of pulses and thus with different duration times ~~, the said pulse groups have the same defined number of pulses~~; and

sending the sequence of pulse groups to a medium;

wherein, at the reception side, the said sequence of pulse groups is received and divided according to the said same defined number;

the ~~d~~ duration ~~uration~~ times of the pulse groups in the sequence of pulse groups are measured and the duration time differences of the pulse groups are used to express ~~the~~ binary digits "0" and "1".

Claim 5 (Original): The digital signal transmission method as set forth in claim 4,

wherein the signals are transmitted within one or multiple sub-channels of the whole bandwidth of the medium; and the said two special frequencies are located in a sub-channel.

Claim 6 (Original): The digital signal transmission method as set forth in claim 5,

wherein each of the said two special frequencies of the pulse groups is located at the each side of the central frequency of the sub-channel.

Claim 7 (Currently amended): The digital signal transmission method as set forth in claim 4,

wherein a synchronous process is included before sending the sequence of pulse groups ~~the normal digit transmission~~ for synchronizing the data transmission and reception and correctly dividing the sequence of pulse groups into the said pulse groups.

Claim 8 (Currently amended): The digital signal transmission method as set forth in claim 7, wherein the said synchronous process is as follows:

a ~~The~~ mark number, a pre-selected multi bytes binary number, is sent from the transmission side repeatedly, and a received number is ~~the signals are~~ received at the signal reception side;

if the received number is not the same with the said mark number, one pulse is canceled before ~~the~~ next time in comparing the received number with the said mark number, until the same number is received.

Claim 9 (Currently amended): A coding circuit for executing the coding method as set forth in claim 1, comprising:

a coding module used for convert the binary digits into a sequence of pulse groups in which the digits "0" and "1" are corresponding to the pulse groups consist of same said defined number of pulses and with two said special defined pulse

frequencies and different duration times; the pulse groups consist of same defined number of pulses; the said defined number is at least 2.

Claim 10 (Previously presented): The coding circuit as set forth in claim 9，wherein said coding module comprising：

an interface, for converting the transmitting digits into serial signals and sending the binary digits logical levels to a voltage level transfer circuit;

a voltage level transfer circuit, for transferring the binary logical levels into two special voltage levels;

a voltage/frequency converter, generating the pulses with said two special defined pulse frequencies according to an input of two said special voltage levels;

a binary counter, for counting the pulses generated by the voltage/frequency converter, and as the said defined number of pulses is counted it controls interface to output the next digit bit.

Claim 11 (Currently amended): A decoding circuit for executing the decoding method as set forth in claim 2 comprising:

a decoding module for dividing said sequence of pulse groups into the pulse groups according to the said same defined number and for measuring the duration time of each pulse group and then converting the said duration time differences into binary digits "0" or "1".

Claim 12 (Previously presented): The decoding circuit as set forth in claim 11, wherein said decoding module comprising:

a binary counter, for counting the pulses in the said sequence of pulse groups, as the said defined number of pulses is reached, it controls the pulse group duration time measurement unit to measure the pulse group duration time;

a pulse group duration time measurement unit, for measuring the duration time of the pulse groups and output "low" or "high" voltage levels according to the difference of the duration time of the pulse groups for expressing the binary digits "0" or "1";

an interface, for receiving the voltage outputs from the pulse group duration time measurement unit, and converting them as the binary logical voltage levels.

Claim 13 (Currently amended): A digital signal transmission circuit, comprising:

a medium for signal transfer;

a coding module at a transmission side, for converting binary digits as a sequence of pulse groups, the binary digits "0" and "1" are corresponding to pulse groups with two special pulse frequencies and with the same defined number of pulses, the pulse groups have the same defined pulses number and <u>different duration times</u> the said defined pulses number is at least two;

a band filer and amplifier module located at a reception side for signal band filtering and amplifying;

a synchronous module, connected with the band filter and amplifier module, for synchronizing the signal transmission and reception, and dividing the said sequence of pulse groups into said pulse groups; and

a decoding module, connected with the synchronous module for dividing the said sequence of the pulse groups into the pulse groups according to the said <u>same</u>

defined number and, for measuring the duration time of each pulse group and then converting the said duration time differences into binary digits "0" or "1".

Claim 14 (Original): The digital signal transmission circuit as set forth in claim 13, wherein said coding module comprising:

a interface, for converting the transmission signal into serial signal and sending the serial logical voltage level to the voltage level transfer circuit;

a voltage level transfer circuit, for converting the serial logical voltage levels into two special voltage levels corresponding to the said two special frequencies;

a voltage/frequency converter, for generating pulses with the said two special frequencies according to the input two special voltage levels and;

a binary counter, for counting the pulses output from the voltage/frequency converter as the said defined number is reached it controls the interface to output another bit.

Claim 15 (Original): The digital signal transfer circuit as set forth in claim 13, wherein said filter and amplifier module comprising filters and amplifiers.

Claim 16 (Original): The digital signal transmission circuit as set forth in claim 13, wherein said synchronous module comprising:

a pulse canceling circuit for each time canceling one pulse;

a comparator, for comparing the number output from decoding module with a said pre-selected mark number, if it is not the same, it controls the pulse canceling circuit to cancel one pulse from the sequence of the pulse groups, whereas if it is the same, the pulse canceling circuit will not work.

Claim 17 (Original): The digital signal transmission circuit as set forth in claim 13, wherein said decoding module comprising:

a binary counter, for counting the pulses in the said sequence of pulse groups; As the said defined number is reached, it controls the pulse group duration time measurement unit to measure the duration time of the pulse groups;

a pulse group duration time measurement unit, for measuring the pulse group duration time and converting the pulse group duration time differences into binary digits "0" and "1".

Claim 18 (Original): The digital signal transmission circuit as set forth in claim 13, wherein said transmission medium is the telephone lines or the electrical cable.

Claim 19 (Original): The digital signal transmission circuit as set forth in claim 13, wherein said transmission medium is electromagnetic wave.